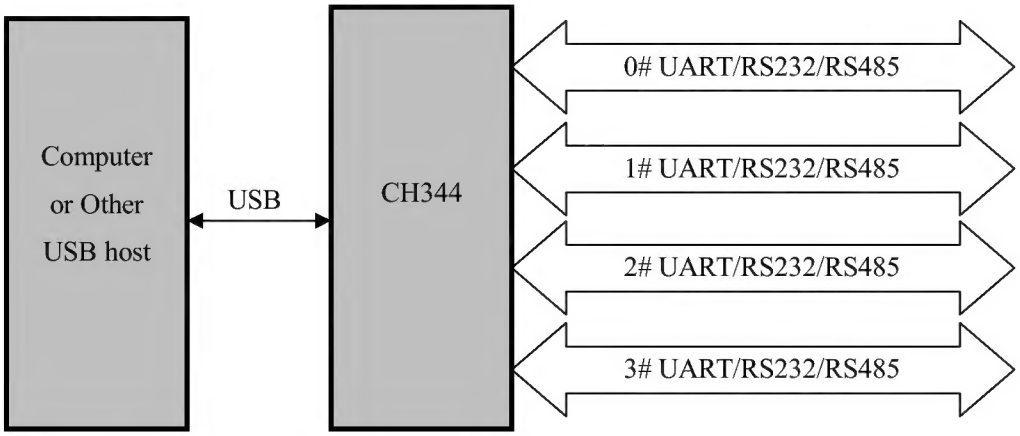
USB to Quad Serial Ports Chip CH344

Datasheet
Version: 1E
http://wch.cn

1. Introduction

CH344 is a USB bus converter chip, which converts USB to quad serial ports UART0/1/2/3, and used to expand serial ports for computer or upgrade directly from normal serial device or MCU to USB bus.



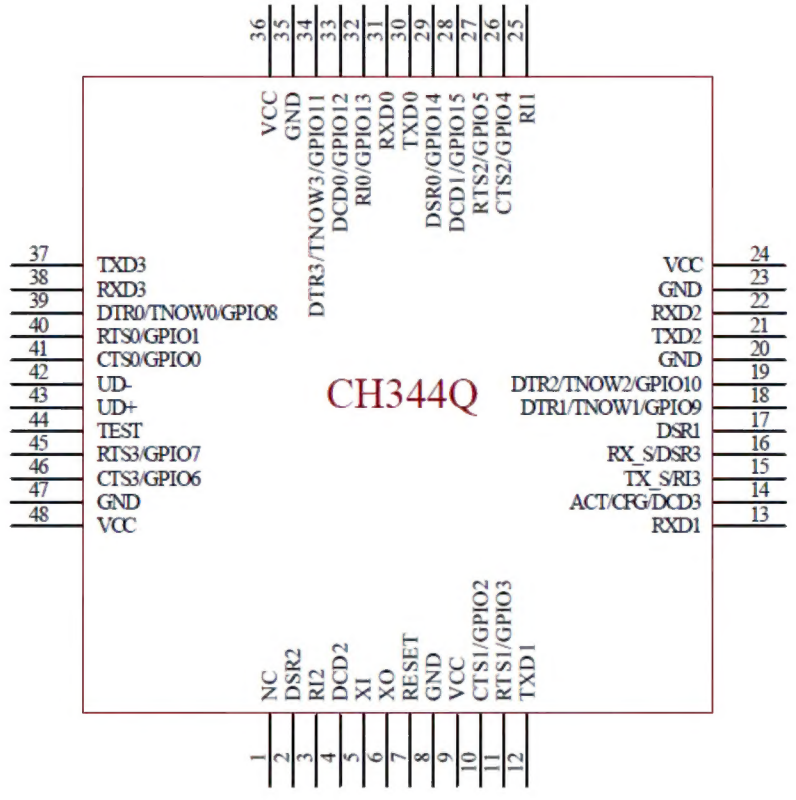
2. Features

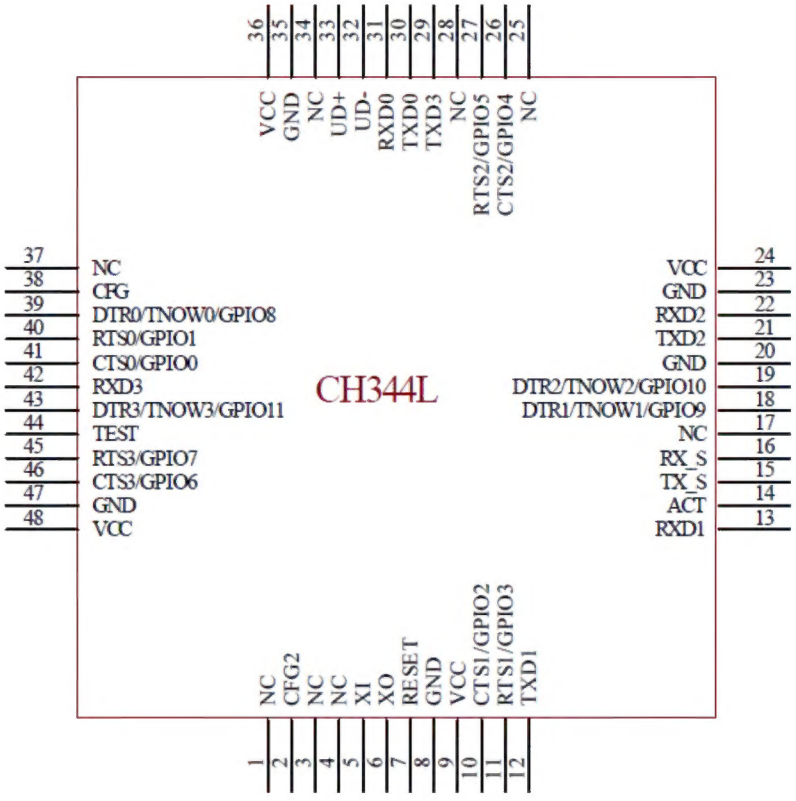
- CH344Q integrates 480Mbps high-speed USB device interface, and CH344L integrates 12Mbps full-speed USB device interface.
- Built-in firmware, emulate standard UART interface, used to upgrade the original serial peripheral or expand additional UART via USB.
- Original serial applications are totally compatible without any modification in Windows operating systems.
- Supports free installation OS which built-in CDC driver or multi-functional high-speed VCP vendor driver.
- Hardware full duplex UART interface, integrated independent transmit-receive buffer.
- CH344Q supports communication baud rate varies from 1200bps to 6Mbps, CH344L supports communication baud rate varies from 1200bps to 230400bps.
- UART supports 8 data bits, and supports odd, even and none parity.
- Integrated 1024-byte RX FIFO and 512-byte TX FIFO for each UART.
- Supports common MODEM signals.
- Supports CTS and RTS hardware automatic flow control.
- Supports half-duplex, provides sending status TNOW, used for controlling RS485 to transmit-receive switch.
- Supports up to 16-channel GPIO input and output function.
- Supports RS232/RS485/RS422 interface, through external voltage conversion chip.
- Built-in EEPROM used to configure the chip of VID, PID, maximum current value, vendor and

product information string, etc.

- Supports only 3.3V power supply.
- RoHS compliant LQFP48 lead-free package.

3. Packages





Package	Body size	Lead pitch		Description	Part No.
LQFP48	7*7mm	0.5mm	19.7mil	Standard LQFP 48-pin patch	CH344Q
LQFP48	7*7mm	0.5mm	19.7mil	Standard LQFP 48-pin patch	CH344L

Note: The USB transceiver of CH344 is designed according to the built-in design of USB2.0, and it is recommended that no external resistor is in series with UD+ and UD- pins.

4. Pin definitions

CH344Q Pin No.	CH344L Pin No.	Pin Name	Pin Type	Pin Description
9,24,36, 48	9,24,36, 48	VCC	POWER	Power supply voltage input, requires an external 0.1uF decoupling capacitor
8,20,23, 35,47	8,20,23, 35,47	GND	POWER	Ground, connected to ground of USB bus directly
7	7	RESET	IN	Input of external reset, active low, built-in pull-up resistor
43	33	UD+	USB signal	Connect to USB D+ Signal directly, do not series resistors
42	32	UD-	USB signal	Connect to USB D- Signal directly, do not series resistors
5	5	XI	IN	Input of crystal oscillator,
6	6	XO	OUT	Inverted output of crystal oscillator
30	30	TXD0	OUT	Transmit asynchronous data output of UART0, high when idle
31	31	RXD0	IN (FT)	Receive asynchronous data input of UART0, built-in pull-up resistor
12	12	TXD1	OUT	Transmit asynchronous data output of UART1, high when idle
13	13	RXD1	IN	Receive asynchronous data input of UART1, built-in pull-up resistor
21	21	TXD2	OUT	Transmit asynchronous data output of UART2, high when idle

22	22	RXD2	IN (FT)	Receive asynchronous data input of UART2, built-in pull-up resistor
37	29	TXD3	OUT	Transmit asynchronous data output of UART3, high when idle
38	42	RXD3	IN (FT)	Receive asynchronous data input of UART3, requires an external pull-up resistor
39	39	DTR0/ TNOW0/ GPIO8	OUT IN(FT)	MODEM output signal of UART0, data terminal ready, active low; RS485 transmit and receive control pin of UART0; General GPIO8, used for IO input or output. CH344Q: During power-on, if it is detected that the pin is connected with a pull-down resistor, it will switch to the TNOW function, otherwise it will be the DTR function; CH344L: During power-on, if it is detected that the CFG2 pin is connected with a pull-down resistor, it will switch to the DTR function, otherwise it will be the TNOW function.
18	18	DTR1/ TNOW1/ GPIO9	OUT IN	MODEM output signal of UART1, data terminal ready, active low; RS485 transmit and receive control pin of UART1; General GPIO9, used for IO input or output. CH344Q: During power-on, if it is detected that the pin is connected with a pull-down resistor, it will switch to the TNOW function, otherwise it will be the DTR function; CH344L: During power-on, if it is detected that the CFG2 pin is connected with a pull-down resistor, it will switch to the DTR function, otherwise it will be the TNOW function
19	19	DTR2/ TNOW2/ GPIO10	OUT IN	MODEM output signal of UART2, data terminal ready, active low; RS485 transmit and receive control pin of UART2; General GPIO10, used for IO input or output. CH344Q: During power-on, if it is detected that the pin is connected with a pull-down resistor, it will switch to the TNOW function, otherwise it will be the

				DTR function; CH344L: During power-on, if it is detected that the CFG2 pin is connected with a pull-down resistor, it will switch to the DTR function, otherwise it will be the TNOW function
34	43	DTR3/ TNOW3/ GPIO11	OUT IN (FT)	MODEM output signal of UART3, data terminal ready, active low; RS485 transmit and receive control pin of UART3; General GPIO11, used for IO input or output. CH344Q: During power-on, if it is detected that the pin is connected with a pull-down resistor, it will switch to the TNOW function, otherwise it will be the DTR function; CH344L: During power-on, if it is detected that the CFG2 pin is connected with a pull-down resistor, it will switch to the DTR function, otherwise it will be the TNOW function
41	41	CTS0/ GPIO0	IN (FT)	MODEM input signal of UART0, clear to send, active low; General GPIO0, used for IO input or output
40	40	RTS0/ GPIO1	OUT	MODEM output signal of UART0, request to send, active low; General GPIO1, used for IO input or output; if RTS0 detects that an external pull-down resistor is connected during power-on, CH344 will disable internal EEPROM configuration parameter and enable chip default parameter
10	10	CTS1/ GPIO2	IN	MODEM input signal of UART1, clear to send, active low; General GPIO2, used for IO input or output
11	11	RTS1/ GPIO3	OUT	MODEM output signal of UART1, request to send, active low; General GPIO3, used for IO input or output,
26	26	CTS2/ GPIO4	IN (FT)	MODEM input signal of UART2, clear to send, active low, General GPIO4, used for IO input or output

27	27	RTS2/ GPIO5	OUT	MODEM output signal of UART2, request to send, active low; General GPIO5, used for IO input or output,
46	46	CTS3/ GPIO6	IN (FT)	MODEM input signal of UART3, clear to send, active low, general GPIO6, used for IO input or output
45	45	RTS3/ GPIO7	OUT	MODEM output signal of UART3, request to send, active low; General GPIO7, used for IO input or output. CH344Q: if RTS3 detects that an external pull-down resistor is connected during power-on, CH344Q will switch PIN14 (ACT/CFG) to DCD3 function, PIN15 (TX_S) to RI3 function, and PIN16 (RX_S) to DSR3 function
14	14	ACT/ CFG/ DCD3	OUT IN	CH344Q: Function 1: USB configuration completion status output, active low, also used as hardware flow control enable pin, active low, built-in pull-up resistor; function 2: MODEM input signal of UART3, data carrier detect, active low. CH344L: USB configuration completed status output, active low
15	15	TX_S/ RI3	OUT IN	CH344Q: Function 1: UART data transmitting status output; Function 2: MODEM input signal of UART3, ring indicator active low. CH344L: UART data transmitting status output
16	16	RX_S/ DSR3	OUT IN	CH344Q: Function 1: UART data receiving status output; Function 2: MODEM input signal of UART3, data set ready, active low. CH344L: UART data receiving status output
	38	CFG	IN	Hardware flow control enable pin, active low, built-in pull-up resistor
44	44	TEST	IN	Internal test pin, an pull-down resistor (usually value is 4.7kΩ) must be connected to ground or connects to ground directly
	2	CFG2	IN	CH344L: TNOW and DTR function configuration pin, optional unified configuration or independent

				configuration. Unified configuration: During power-on, if CFG2 pin detects high level or not connected, all DTRx/TNOWx pins are configured to function as TNOW. CFG2 pin is low, all DTRx/TNOWx pins are configured for DTR function. Independent configuration: During power-on, the CFG2 pin is connected to a low level and needs to be configured as a UART for the TNOW function. Then, connect a pull-down resistor (such as 4.7KΩ) to the DTRx/TNOWx pin of the corresponding UART to the ground. If the pin is not connected to the pull-down resistor, configure the DTR function.
33		DCD0/ GPIO12	IN (FT)	MODEM Input signal of UART0, data carrier detect, active low; General GPIO12, used for IO input or output
32		RI0/ GPIO13	IN (FT)	MODEM Input signal of UART0, ring indicator, active low; General GPIO13, used for IO input or output
29		DSR0/ GPIO14	IN (FT)	MODEM Input signal of UART0, data set ready, active low; General GPIO14, used for IO input or output
28		DCD1/ GPIO15	IN (FT)	MODEM Input signal of UART1, data carrier detect, active low; General GPIO15, used for IO input or output
25		RI1	IN (FT)	MODEM Input signal of UART1, ring indicator, active low
17		DSR1	IN	MODEM Input signal of UART1, data set ready, active low
4		DCD2	IN	MODEM Input signal of UART2, data carrier detect, active low
3		RI2	IN	MODEM Input signal of UART2, ring indicator, active low
2		DSR2	IN	MODEM Input signal of UART2, data set ready, active low

1	1,3,4,17, 25,28,34, 37	NC	None	No connection, do not connect

Note: CH344Q: FT means the pin can tolerate 5V voltage when used as input.

5. Function descriptions

5.1. General description

CH344 supports 3.3V supply voltage, the power pin should be respectively connected to an external power decoupling capacitor of about 0.1uF.

CH344 has integrated power-on reset circuit. When the chip is operating, it needs to provide an external 8MHz clock signal to the XI pin. The clock signal can be generated by the built-in inverter of CH344 through crystal frequency stabilization oscillation. The peripheral circuit needs to connect an 8MHz crystal between the XI and XO pins, and the both pins connect to the ground with an oscillation capacitor of about 20pF. It is recommended to use an external 8MHz crystal.

For CH344L, it is recommended to use an external crystal. If the chip's operating environment is relatively ideal, it is not need to solder the external crystal, and the chip will automatically switch to use the built-in crystal.

CH344 has built-in all the peripheral circuits required by the USB bus, including the embedded USB controller and USB-PHY, the series matching resistor of the USB signal line, and the 1.5K pull-up resistor required by the Device. The UD+ and UD- pins can be directly connected to PC or other USB host. If a fuse resistor or inductor or ESD protection device is connected in series for chip safety, then the AC and DC equivalent series resistor should be within 5Ω.

5.2. UART description

CH344 provides quad serial ports UART0/1/2/3, each UART includes TXD, RXD, CTS and RTS pin, etc. CH344Q also provides MODEM signals such as DCD, RI and DSR, it can realize 3-line UART, 5-line or 9-line UART communication.

In UART mode, CH344 contains: data transfer pins, MODEM interface signal pins and assistant pins.

Data transfer pins contain: TXD0, RXD0, TXD1, RXD1, TXD2, RXD2, TXD3 and RXD3, RXDx is high when UART transmission is idle. TXDx is high when UART reception is idle.

MODEM interface signal pins contain: CTS0, RTS0, DTR0, DCD0, RI0, DSR0, CTS1, RTS1, DTR1, DCD1, RI1, DSR1, CTS2, RTS2, DTR2, DCD2, RI2, DSR2, CTS3, RTS3, DTR3, DCD3, RI3, DSR3.

Assistant pins contain: ACT, TX_S, RX_S, TNOW0, TNOW1, TNOW2, TNOW3, CFG and CFG2, etc. The ACT is the output pin of USB device configuration completion status. The default outputs high level during power-on and outputs low level after the USB host performs USB configuration on CH344. TX_S is the output pin of the chip's serial UART sending data status. When any serial UART is sending data, TX_S outputs a pulse level with a period of 200mS. RX_S is the output pin of the chip's serial UART receiving data status. When any serial UART is receiving data, the RX_S outputs a pulse level with a period of 200mS. TNOWx is the RS485 sending and receiving control pin of the corresponding serial UART. The ACT pin of CH344Q (CFG pin of CH344L) is the hardware automatic flow control configuration pin. The chip detects

the level status of this pin when power-on. If it is not connected or inputs high level, hardware flow control will not be enabled; inputs low level will enable hardware flow control.

The CFG2 pin of the CH344L is the TNOW and DTR function configuration pins, which can be either unified configuration or independent configuration.

Unified configuration: During power-on, if the CFG2 pin is at a high level or not connected, all DTRx/TNOWx pins are configured to function as TNOW. CFG2 pin is low, all DTRx/TNOWx pins are configured for DTR function.

Independent configuration: During power-on, the CFG2 pin is connected to a low level and needs to be configured as a UART for the TNOW function. Then, connect a pull-down resistance (such as 4.7KΩ) to the DTRx/TNOWx pin of the corresponding UART to the ground. If the pin is not connected to the pull-down resistance, configure the DTR function.

The RTS3 pin of the CH344Q is the MODEM signal enable pin of the UART3 part. During power-on, if the RTS3 pin detects an external pull-down resistor, switch PIN14 (ACT/CFG) to DCD3 function, PIN15 (TX_S) to RI3 function, and PIN16 (RX_S) to switch to DSR3 function.

Each UART of CH344 has built-in independent transmit-receive buffer, supports simplex, half-duplex and full-duplex asynchronous serial communication.

CH344Q is based on USB high-speed 480Mbps, the serial data of UART0/1/2/3 contains a low-level start bit, 8 data bits and 1/2 high-level stop bits, supports none/odd/even parity. The common communication baud rate: 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 460800, 921600, 1M, 1.5M, 2M, 3M, 4M, 5M, 6M, etc.

CH344L is based on USB full-speed 12Mbps, the serial data of UART0/1/2/3 contains a low-level start bit, 8 data bits and 1/2 high-level stop bits, supports none/odd/even parity. The common communication baud rate: 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, etc. If the baud rate is set to higher, 4 serial ports may not support bidirectional communication at the same time.

Quad UARTs of CH344 all support CTSx and RTSx hardware automatic flow control, which can be enabled or disabled (default) at the same time by ACT/CFG configuration and can be independently configured through the VCP vendor driver. If enabled, UART only will continue to send the next data when CTSx input is valid (active low), otherwise the UART transmission will be stopped; UART will automatically set RTSx to be valid (active low) when the receiving buffer is empty, it will automatically invalidate RTSx until the data in the receiving buffer is nearly full, and RTSx will be valid again when the buffer is empty. While using hardware automatic flow control, CTSx of CH344 should connect to RTSx of the counterpart, and RTSx of CH344 should connect to CTSx of the counterpart.

The allowable baud rate error of CH344's serial UART receiving signal is less than 2%, the baud rate error of serial UART transmitting signal is less than 1.5%.

In the Windows OS, CH344 supports CDC driver that comes with system, and can install high-speed VCP vendor driver. It can emulate standard serial UART, so the mostly original serial applications are totally compatible, without any modification. In VCP vendor driver mode, it can support up to 16-channel GPIO input and output function.

CH344 can be used to upgrade the original serial peripheral devices, or expand extra serial ports for

computers via USB bus. Through external level shifting chip provides RS232, RS485, RS422 and other interfaces can be further.

5.3. Parameter configuration

In larger batch applications, the vendor identification code (VID) and product identification code (PID) of CH344 and product information can be customized.

In less batch applications, parameters can be configured by built-in EEPROM. After installs VCP vendor driver, through configuration tool CH34xSerCfg.exe provided by chip manufacturer, it can be flexibly configured the identification code (VID), product identification code (PID), maximum current value, BCD version number, manufacture information and product information string and other descriptor, etc.

6. Parameters

6.1. Absolute maximum ratings

(Operating in critical ratings or exceeding the absolute maximum ratings may cause chip to not work or even be damaged)

Symbol	Parameter Description	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-40	105	℃
VCC	Supply voltage(VCC connects to power, GND connects to ground)	-0.3	4.0	V
VUSB	USB signal voltage	-0.5	3.8	V
VIO5V	5V tolerant on the UART pins	-0.5	5.6	V
VUART	UART and others voltage	-0.5	VCC+0.3	V

6.2. Electrical characteristics

(Test conditions: TA=25℃,VCC =3.3V, exclude USB pin)

Symbol	Parameter Description		Min.	Typ.	Max.	Unit
VCC	Supply voltage (VCC power supply, GND connects to ground)		3.0	3.3	3.6	V
ICC	Operating supply current	CH344Q	27	37	50	mA
		CH344L	12	18	24	mA
ISLP	The supply current when USB is suspended	CH344Q	160	230	320	uA
		CH344L	200	450	600	uA
VIL	Input low voltage		0		0.8	V

VIH	Input high voltage		2.0		VCC	V
VIH5	Tolerate high level input voltage for 5V pins		2.0		5.0	V
VOL	Output low voltage, single pin 8mA sunk current				0.4	V
VOH	Output high voltage, single pin outputs 8mA current		VCC-0.4			V
RPU	Built-in pull-up equivalent resistance		30	40	60	KΩ
VPOR	Threshold voltage for power on/ power off reset		1.9	2.2	2.5	V
VESD	ESD electrostatic discharge voltage (mannequin, non-contact)	CH344Q	4			KV
		CH344L	2			KV

6.3. Timing parameters

(Test conditions: TA=25℃, VCC= 3.3V)

Symbol	Parameter Description		Min.	Typ.	Max.	Unit
FD	CH344L Error of internal clock (influence baud rate comparatively)	TA=0℃～70℃	-1.5	0.8	1.5	%
		TA=-40℃～85℃	-2	1.5	2	%
TRSTD	Reset delay after power-on or external reset input		15	30	45	mS
TSUSP	Detect USB automatic suspend time		3	5	9	mS
TWAKE	Wake-up completion time after chip sleep		0.3	0.5	4	mS

7. Application

7.1. USB to 4-channel TTL UART

The image below shows that CH344Q converts USB to 4-Channel TTL UART. The signal line in the image can only be connected to RXDx, TXDx and public ground. CTSx, RTSx, TNOWx can be selected as needed, and all can be not connected when not needed.

P1 is USB port, USB bus contains a pair of 5V power lines and a pair of data signal lines. Usually, the color of +5V power line is red, the black is ground. D+ signal line is green and the D- is white. The supply current provided by USB bus can up to 500mA.

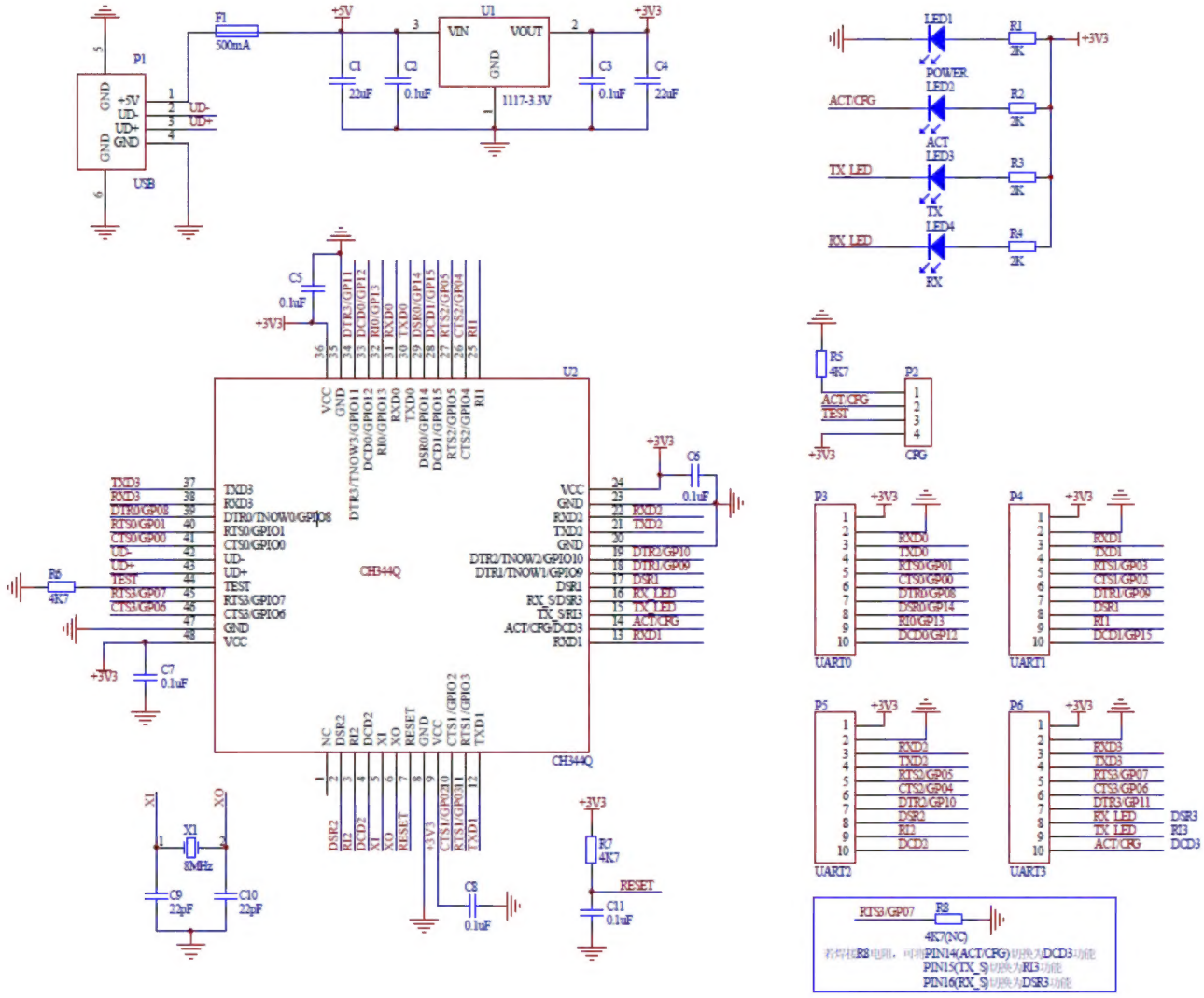
P3, P4, P5, and P6 are the TTL connection pins of each serial UART, including: VCC, GND, RXDx, TXDx, RTSx, CTSx, and TNOWx, etc. Level conversion chip can be added to realize signal conversion from TTL to RS232, RS485, RS422, etc.

CH344Q supports 3.3V supply voltage. Each power pin should be connected to a power decoupling capacitor with a capacity of about 0.1uF. In the image, C5, C6, C7 and C8 are power decoupling capacitors. R7 and C11 are optional devices.

Crystal X1, capacitors C9 and C10 are used in the clock oscillation circuit of CH344Q. The frequency of X1 is 8MHz±0.4‰, C9 and C10 are monolithic or high-frequency ceramic capacitors with a capacity of about

22pF. For CH344L, the crystal and capacitance can be saved as needed, but the baud rate error is slightly larger.

It is recommended to add ESD protection device for USB signal line. The parasitic capacitance of ESD chip should be less than 2pF, such as ch412k.

It is recommended that the serial port peripherals and the CH344 use the same power supply. Otherwise, the I/O pin reverse current when the serial port peripherals are powered separately must be considered.

When designing the PCB, pay attention to: decoupling capacitor C5,C6,C7 and C8 get as close to the connected power pin of CH344 as possible; Enabling the D+ and D- signal lines of USB port close to the parallel wiring, and providing ground or copper on both sides to reduce signal interference from the outside.